What is claimed:

1. A semiconductor device comprising a memory cell area and a semiconductor circuit section other than the memory cell section that are formed on the same semiconductor substrate, the memory cell section having a plurality of memory cells each of which includes a first driver transistor, a second driver transistor, a first load transistor, a second load transistor, a first transfer transistor, and a second transfer transistor, wherein:

each of the memory cells comprises a first gate electrode layer, a second gate electrode layer, a first drain-drain contact layer, a second drain-drain contact layer, a first drain-gate contact layer, and a second drain-gate contact layer;

the first gate electrode layer comprises a gate electrode of the first driver transistor and a gate electrode of the first load transistor;

the second gate electrode layer comprises a gate electrode of the second driver transistor and a gate electrode of the second load transistor;

the first drain-drain contact layer and the second drain-drain contact layer are located above the first gate electrode layer and the second gate electrode layer;

the first drain-drain contact layer is used to connect a drain region of the first driver transistor to a drain region of the first load transistor;

the second drain-drain contact layer is used to connect a drain region of the second driver transistor to a drain region of the second load transistor;

the first drain-gate contact layer is located above the first drain-drain contact layer and the second drain-drain contact layer;

the first drain-gate contact layer is used to connect the first drain-drain contact layer to the second gate electrode layer;

the second drain-gate contact layer is used to connect the second drain-drain contact layer to the first gate electrode layer; and

the semiconductor circuit section has no wiring layer at the same level as the first drain-drain contact layer and the second drain-drain contact layer.

2. The semiconductor device according to claim 1, wherein a thickness of the first drain-drain contact layer and the second drain-drain contact layer is 100 nm to 170 nm.

3. The semiconductor device according to claim 1, wherein the first drain-drain contact layer and the second drain-drain contact layer comprise a refractory metal nitride layer.

4. The semiconductor device according to claim 1, further comprising a field effect transistor, a first interlayer dielectric, a second interlayer dielectric, a wiring layer, and

a contact-conductive section, wherein:

the field effect transistor is located in the semiconductor circuit section;

the first interlayer dielectric is located in the memory cell section so as to cover the first gate electrode layer and the second gate electrode layer;

the first interlayer dielectric is located in the semiconductor circuit section so as to cover a gate electrode of the field effect transistor,;

the second interlayer dielectric is formed in the memory cell section so as to cover the first drain-drain contact layer and the second drain-drain contact layer;

the second interlayer dielectric is located on the first interlayer dielectric in the semiconductor circuit section;

the wiring layer is located on the second interlayer dielectric in the semiconductor circuit section;

the wiring layer is located at the same level as the first drain-gate contact layer and the second drain-gate contact layer;

the contact-conductive section is located in a hole section formed through the first interlayer dielectric and the second interlayer dielectric in the semiconductor circuit section; and

the contact-conductive section is used to connect the wiring layer to at least one of a source/drain of the field effect transistor and a gate electrode of the field effect transistor.

5. The semiconductor device according to claim 4, wherein an aspect ratio of the hole section is 5 or less.

6. The semiconductor device according to claim 1, wherein the semiconductor circuit section comprises a logic circuit section.

7. The semiconductor device according to claim 1, wherein the first gate electrode layer, the second gate electrode layer, the first drain-drain contact layer, and the second drain-drain contact layer respectively have a linear pattern and are disposed in parallel one another.

8. The semiconductor device according to claim 1, wherein:

the first driver transistor and the second driver transistor are n-type;

the first load transistor and the second load transistor are p-type;

the first transfer transistor and the second transfer transistor are n-type;

the memory cell section comprises a first conductive layer, a second conductive layer, a third conductive layer, and a fourth conductive layer;

the first gate electrode layer, the second gate electrode layer, and a sub-word line are located in the first conductive layer;

the first drain-drain contact layer, the second

drain-drain contact layer, a power supply line, a first contact pad layer, a second contact pad layer, and a third contact pad layer are located in the second conductive layer;

the first drain-gate contact layer, the second drain-gate contact layer, a main-word line, a fourth contact pad layer, a fifth contact pad layer, and a sixth contact pad layer are located in the third conductive layer;

a first bit line, a second bit line, and a ground line are located in the fourth conductive layer;

the sub-word line extends in a first direction;

the power supply line is connected to a source region of the first load transistor and the second load transistor;

the first contact pad layer is used to connect the first bit line to a source/drain region of the first transfer transistor;

the second contact pad layer is used to connect the second bit line to a source/drain region of the second transfer transistor;

the third contact pad layer is used to connect a source region of the first driver transistor and the second driver transistor to the ground line;

the main-word line extends in the first direction;

the fourth contact pad layer is used to connect the first bit line to a source/drain region of the first transfer transistor;

the fifth contact pad layer is used to connect the second bit line to a source/drain region of the second transfer

transistor;

the sixth contact pad layer is used to connect a source region of the first driver transistor and the second driver transistor to the ground line; and

the first bit line and the second bit line extend in a second direction which intersects the first direction at right angles.

9. The semiconductor device according to claim 1, wherein a size of the memory cell is 4.5 μm^2 or less.